IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method of data access, said method comprising:
precharging a first bitline and a second bitline;
permitting charge sharing between a capacitance of a memory cell and ~~the precharged first bitline~~ one of the precharged first bitline and the precharged second bitline;
biasing ~~the precharged second bitline~~ the other of the precharged first bitline and the precharged second bitline; and
subsequent to said permitting charge sharing and said biasing, sensing a difference between a potential of the first bitline and a potential of the biased second bitline.

2. (Original) The method according to claim 1, wherein said biasing includes altering a potential of the second bitline.

3. (Original) The method according to claim 1, wherein said biasing includes reducing a potential of the second bitline.

4. (Original) The method according to claim 1, wherein sensing a difference between a potential of the first bitline and a potential of the second bitline includes amplifying said difference.

5. (Original) The method according to claim 1, wherein said permitting charge sharing includes applying a potential to a gate of a transistor of the memory cell.

6. (Original) The method according to claim 1, wherein said biasing includes applying a potential to a bias capacitor coupled to the second bitline.

7. (Currently amended) A method of data access, said method comprising:
selecting a wordline;
asserting a bias signal corresponding to the wordline; and

sensing a difference between a potential of a bitline coupled to the wordline and a potential of a reference bitline,

wherein charge sharing between a memory cell and the bitline coupled to the wordline occurs as a consequence of said selecting a wordline, and

wherein the potential of the reference bitline is altered as a consequence of said asserting a bias signal.

8. (Original) The method according to claim 7, wherein said asserting a bias signal occurs subsequent to said selecting a wordline.

9. (Currently amended) The method according to claim 7, wherein said sensing a difference includes sensing a difference between the potential of the bitline and the altered potential of the reference bitline.

10. (Original) The method according to claim 7, wherein the potential of the reference bitline is reduced as a consequence of said asserting a bias signal.

11. (Original) A method of data access, said method comprising:

precharging a first bitline and a second bitline;

permitting charge sharing between a capacitance of a memory cell and the precharged first bitline;

biasing a selected one of the precharged bitlines; and

subsequent to said permitting charge sharing and said biasing, sensing a difference between a potential of the first bitline and a potential of the second bitline.

12. (Original) The method according to claim 11, wherein said biasing includes altering a potential of the selected bitline.

13. (Original) The method according to claim 11, wherein said biasing includes applying a potential to a bias capacitor coupled to the selected bitline.

14. (Currently amended) A ~~storage~~ semiconductor memory device comprising:

a precharging circuit configured and arranged to precharge a bitline and a reference

bitline;

a memory cell configured and arranged to share charge with the bitline;

a bias circuit configured and arranged to ~~alter~~ bias a potential of the reference bitline to increase a refresh period in a semiconductor memory device; and

a sense amplifier configured and arranged to sense a difference between a potential of the bitline and a potential of the reference bitline.

15. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 14, wherein the memory cell includes a field-effect transistor and a capacitor.

16. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 14, wherein the memory cell is coupled to a wordline and is further configured and arranged to share charge with the bitline upon a predetermined alteration in a potential of the wordline.

17. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 14, wherein the bias circuit is configured and arranged to reduce a potential of the reference bitline.

18. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 14, wherein the bias circuit includes a bias capacitor coupled to the reference bitline.

19. (Currently amended) The ~~storage~~ semiconductor memory device according to claim ~~14~~ 18, wherein the bias capacitor includes a metal-oxide-semiconductor field-effect transistor having a low threshold voltage.

20. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 19, wherein a magnitude of the threshold voltage of the metal-oxide-semiconductor field-effect transistor is less than three hundred millivolts.

21. (Currently amended) The ~~storage~~ semiconductor memory device according to claim ~~14~~ 18, wherein the bias capacitor includes an n-channel metal-oxide-semiconductor field-effect transistor having a low threshold voltage.

22. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 21, wherein a magnitude of the threshold voltage of the metal-oxide-semiconductor field-effect transistor is less than three hundred millivolts.

23. (Currently amended) The ~~storage~~ semiconductor memory device according to claim 14, further comprising:

a second memory cell configured and arranged to share charge with the bitline;

a first isolation circuit configured and arranged to isolate the memory cell from the sense amplifier; and

a second isolation circuit configured and arranged to isolate the second memory cell from the sense amplifier.